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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/578,028

04/27/2006

Kyoung-Ju Shin

AB-1883 US

9578

32605

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04/01/2009

Haynes and Boone, LLP

IP Section

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EXAMINER

NGUYEN, THANH NHAN P

ART UNIT

PAPER NUMBER

2871

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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/578,028	<b>Applicant(s)</b> SHIN ET AL.	
	<b>Examiner</b> THANH-NHAN P. NGUYEN	<b>Art Unit</b> 2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 16 December 2008.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5 and 8-12 is/are rejected.
- 7) ☒ Claim(s) 6,7,13 and 14 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 April 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## DETAILED ACTION

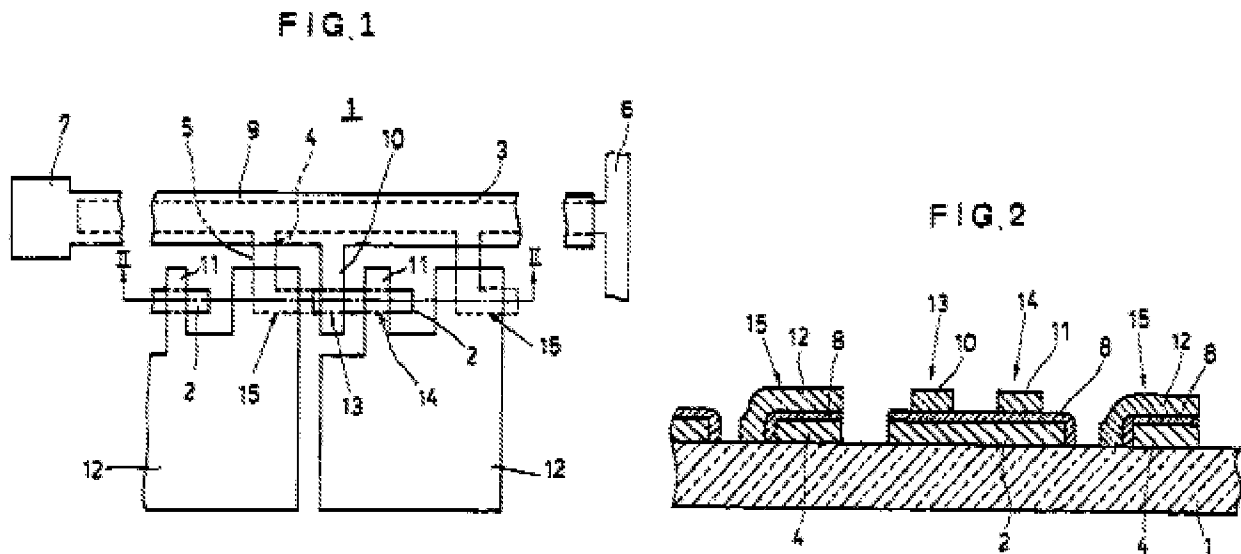
### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**Claims 1-5 and 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sekiguchi (US 5893621) in view of Den Boer et al (US 6,243,062).**

Sekiguchi discloses (Figs. 1 and 2) a thin film diode array panel comprising:



Claims 1 and 2:

- an insulating substrate (1)

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- first redundant gate lines (3) made of an opaque conductor and formed on the insulating substrate
- first floating electrodes (2) made of an opaque conductor, formed on the insulating substrate, and disposed between the first and second redundant gate lines
- an insulating layer (8) formed on the first floating electrodes
- a first gate line (9) formed at least partially directly on the first redundant gate line (3) and including a first input electrode (10) overlapping the first floating electrode (2) where the insulating layer (8) is interposed between the first input electrode and the first floating electrode
- a pixel electrode (12) including a first contact electrode (11) overlapping the first floating electrode (2) where the insulating layer (8) is interposed between the first contact electrode and the first floating electrode, and a main body
- wherein the pixel electrode (12) and the first gate line are made of indium tin oxide (col. 10, lines 35-38)

Sekiguchi lacks disclosure of:

- second redundant gate lines made of an opaque conductor and formed on the insulating substrate; wherein the first and second redundant gate lines made of Mo
- a second floating electrode made of an opaque conductor
- an insulating layer formed on the second floating electrodes

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- a second gate line formed at least partially directly on the second redundant gate line and including a second input electrode overlapping the second floating electrode where the insulating layer is interposed between the second input electrode and the second floating electrode
- a second contact electrode overlapping the second floating electrode where the insulating layer is interposed between the second contact electrode and the second floating electrode

In summary, Sekiguchi discloses a MIM instead of a dual MIM as the present invention claims.

However, it was well known in the art to use a dual MIM diode for the benefit of improving response time and reducing the potential for crosstalk or image retention, as evidenced by Den Boer et al, (Fig. 6; Abstract; col. 12, lines 11-66; col. 13, lines 1-67).

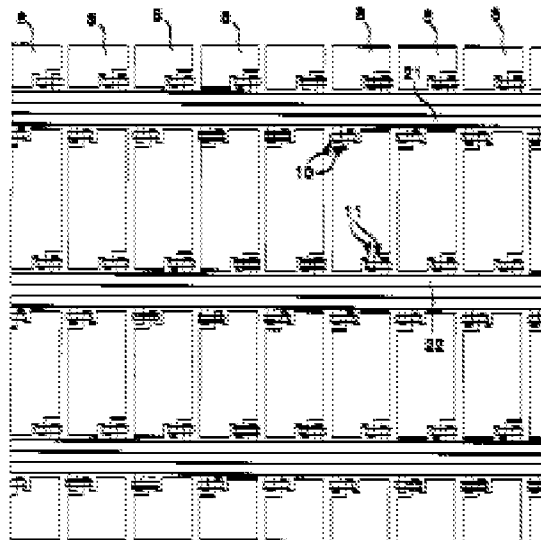


FIG. 6

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Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use a dual MIM diode for the benefit of improving response time and reducing the potential for crosstalk or image retention.

Claim 3:

- wherein the insulating layer (8) includes a first insulating layer regionally formed around the first floating electrode (2)

From the rejection above as in claim 1, it would have been obvious to have a second insulating layer regionally formed around the second floating electrode; thus, it does not patentably distinguish the invention.

Claims 4 and 5:

Sekiguchi discloses all limitations as in claim 1.

Further, similarly, from the rejection as in claim 1, it would have been obvious to have the insulating layer covers the first and second redundant gate lines and the first and second floating electrodes and has contact holes exposing the first and second redundant gate lines.

Sekiguchi lacks disclosure of the first and second gate lines are connected to the first and second redundant gate lines through the contact holes; the insulating layer covers the first and second redundant gate lines and the first and second floating electrodes and has cutout stripes exposing the first and second redundant gate lines, and the first and second gate lines are connected to the first and second redundant gate lines through the cutout stripes.

However, it would have been obvious to one of ordinary skill in the art to have the gate lines and the redundant gate lines connected through the contact hole or through the cutout stripes of the insulating layer, at least for the benefit of obtaining more secure/contact between the two layers/two lines.

Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have the gate lines and the redundant gate lines connected through the contact hole or through the cutout stripes of the insulating layer, at least for the benefit of obtaining more secure/contact between the two layers/two lines.

Claims 8-12 are met the discussion regarding claims 1-5 rejection above, respectively.

***Allowable Subject Matter***

Claims 6, 7, 13 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reason for allowance: There is no prior art of record that teaches or suggests a thin film diode array panel comprising a relationship of various elements as claimed with the specific allowable subject matter cited in the following claims:

Claims 6 and 13:

- wherein the insulating layer has a cutout disposed to overlap at least a portion of the main body of the pixel electrode

Claim 7 is allowed since it depends on allowed claim 6.

Claim 14 is allowed since it depends on allowed claim 13.

***Response to Arguments***

Applicant's arguments with respect to claims 1-5 and 8-12 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 6593991.

2. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.



***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to (Nancy) Thanh-Nhan P. Nguyen whose telephone number is 571-272-1673. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

-- March 26, 2009

TN

/David Nelms/

Supervisory Patent Examiner, Art Unit 2871